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PN - JP6120985 A 19940428
 TI - PACKET LINE BACKUP SYSTEM
 FI - H04L1/22 ; H04L11/20&102Z ; H04Q11/04&M
 PA - OKI ELECTRIC IND CO LTD
 IN - CHIMURA YASUBUMI
 AP - JP19920267245 19921006
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AN - 1994-180327 [22]
 TI - Packet switching with built-in redundancy - incorporates built-in redundancy in packet switching to eliminate communications interruptions during changeovers
 AB - J06120985 The packet switch comprises the packet switchers (110,120) forming switcher A and switcher B, the latter being a back up. The two switchers are connected to a common bus (130). A protocol processors module (140) carries out multiple link processing with assistance of a controller (150) to assist switch-over of the traffic channel from A to B when the former becomes defective or exhibits an error.
 - The layer no.3 controller (440) enables the set changeover to channel B and activates layer no.2 controller (420) using a multi-link controller (430) in accordance with the logic path.
 - ADVANTAGE - Back up channel arrangement of packet switch provides redundancy. Changeover does not interrupt on chop, smooth flow of communication signal; entire processing is carried out in real time.
 - (Dwg.1/3)
 IW - PACKET SWITCH BUILD REDUNDANT INCORPORATE BUILD REDUNDANT PACKET SWITCH ELIMINATE COMMUNICATE INTERRUPT CHANGEOVER
 PN - JP6120985 A 19940428 DW199422 H04L12/56 008pp
 IC - H04L1/22 ;H04L12/56 ;H04Q11/04
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 TI - PACKET LINE BACKUP SYSTEM
 AB - PURPOSE:To switch lines without interrupting communication in the case of switching a line directly connecting devices and being normally used to a backup line through a line exchange network.
 - CONSTITUTION:Line housing circuits 110 and 120 housing respectively packet lines A and B are connected by a common bus 130, to which a protocol processing circuit 140 performing the multilink processing of the packets to respective lines A and B and a line controlling device 150 performing a call setting processing from the backup line B are connected. In the processing circuit 140, the fault generation and recovery from the fault of the packet line A are detected, which are notified to the line control circuit 150 to perform the call setting and release from the line B. Then, in a layer 3 control section 440, the logic path selecting respective lines A and B is set. According to the logic path, they are distributed into layer 2 control sections 410 and 420 in a multilink control section 430 and the transmission is performed through the housing circuits 110 and 120 of the lines A and B.
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